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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,503	10/25/2001	Katsuji Iguchi	SLA0636	3213

7590 03/06/2003

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EXAMINER
LATTIN, CHRISTOPHER W

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/035,503	Applicant(s) IGUCHI ET AL.	
	Examiner Christopher W Lattin	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 1 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6, 11, 15, 17 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Szluk et al. (U.S. Patent 4,703,551).

Szluk et al. teach a method of forming a MOS device on a silicon substrate 10, comprising preparing a substrate to contain a conductive region 13 of a first conductivity type having a first device active area; forming a gate electrode structure on the first device active area, said gate electrode structure including a gate electrode 16p and insulating sidewalls 29p; implanting ions of an opposite conductivity type from that of said first device active area into the exposed portions of said conductive region to form source and drain regions 27p and 28p on opposite sides of said gate structure; and depositing by selective CVD a silicide layer 41p, 42p, and 46p over said source and drain regions and over said gate electrode. See especially column 9 line 61- column 10 line 7.

With reference to claims 11, 15, 17 and 21, Szluk et al. teach a method of forming a CMOS device on a silicon substrate, comprising: preparing a substrate 10 to contain a conductive region 13 of a first type having a first device active area therein,

and to contain a conductive region of a second type 10 having a second device active area therein; forming gate electrodes 16 on the first and on the second active areas; depositing and forming a gate electrode sidewall insulator 21 layer on each gate electrode; masking the first device active area; implanting ions of a first type into the exposed portions of the second device active area to form a source region 27n and a drain region 28n in the second device active area; stripping the mask 26; masking the second device active area; implanting ions of a second type into the exposed portions of the first device active area to form a source region 27p and a drain region 28p in the first device active area; stripping the mask 36; and depositing a silicide layer 41p, 42p, and 46p by CVD over the gate electrodes and the source and drain region in the first and second device active areas.

Claims 11, 16, 17 and 22 rejected under 35 U.S.C. 102(b) as being anticipated by Tsai et al. (U.S. Patent 5,757,045).

Tsai et al. teach a method of forming a CMOS device on a silicon substrate, comprising: preparing a substrate 1 to contain a conductive region 7 of a first type having a first device active area therein, and to contain a conductive region of a second type 10b having a second device active area therein; forming gate electrodes 12 on the first and on the second active areas; depositing and forming a gate electrode sidewall insulator 14 layer on each gate electrode; masking the first device active area; implanting ions of a first type into the exposed portions of the second device active area to form a source region 16 and a drain region 16 in the second device active area;

stripping the mask 15; masking the second device active area; implanting ions of a second type into the exposed portions of the first device active area to form a source region 18 and a drain region 18 in the first device active area; stripping the mask 17; depositing a silicide layer 19 over the gate electrodes and the source and drain region in the first and second device active areas and depositing an insulating layer 29 over the structure and metallizing the structure with layer 29.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 7-9, 12-14 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Szluk et al. (U.S. Patent 4,703,551) in view of Wu (U.S. Patent 6,069,044).

Szluk et al. are applied supra and teach all of the limitations of the presently claimed method, but fail to teach low energy plasma immersion techniques for ion implantation. Wu teach a method of implanting ions using plasma immersion ion implantation at an energy in the range of about 0.5 keV to 2 keV and a dose in a range of about $10x10^{14}$ cm^{-2} to $10x10^{15}$ cm^{-2} (which corresponds to a concentration $10x10^{19}$ cm^{-3} to $10x10^{22}$ cm^{-3}) in order to form shallow junction regions. It would have been obvious to one skilled in the art at the time of the invention to implant using plasma

immersion ion implantation and the parameters indicated to form shallow junction regions that can perform at high speeds.

Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Szluk et al. (U.S. Patent 4,703,551) in view of Tsai et al. (U.S. Patent 5,757,045). Szluk et al. are applied supra to claims 1 and 6 and teach all of the limitations of the presently claimed method, but fail to teach depositing an insulating layer over the structure and metallizing the structure. Tsai et al. teach that it is well known to form an insulating layer and metallizing the structure to form connections to the device. It would have been obvious to one skilled in the art at the time of the invention to form an insulating layer and metallizing the structure in order to form electrical connections for the device.

Double Patenting

Claim 6 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 1. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Lattin whose telephone number is (703) 305-3017. The examiner can normally be reached Monday through Friday from 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached at (703) 308-3325. The fax numbers for this Group are (703) 872-9318 for responses to non-final actions and (703) 872-9319 responses to final actions.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

CWL
February 28, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800